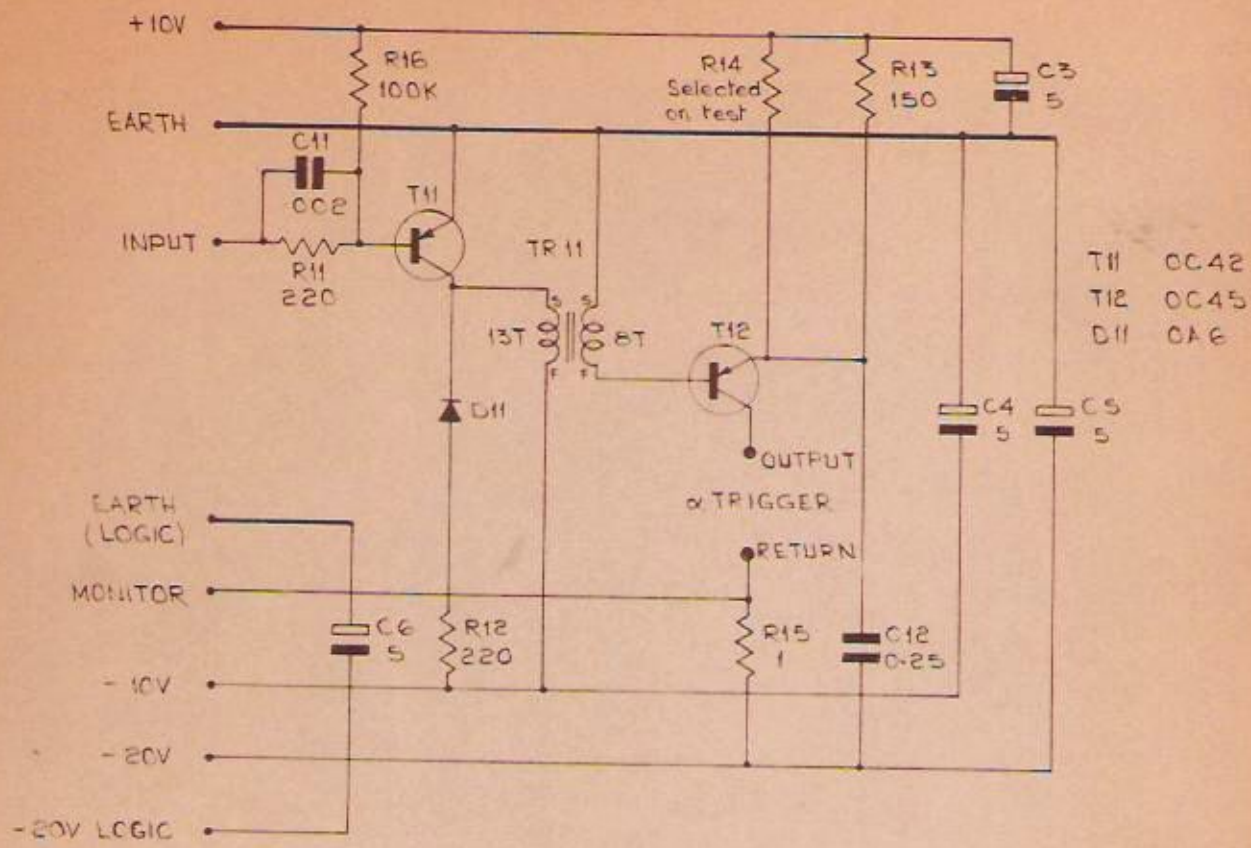
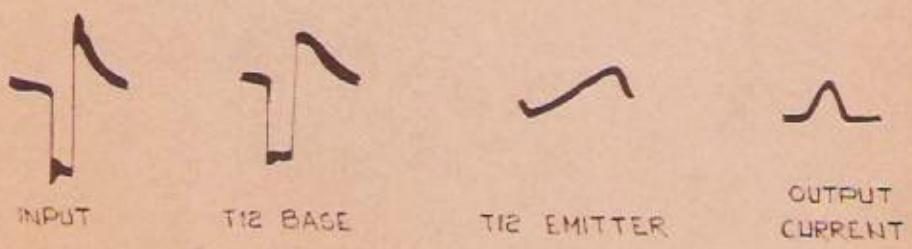


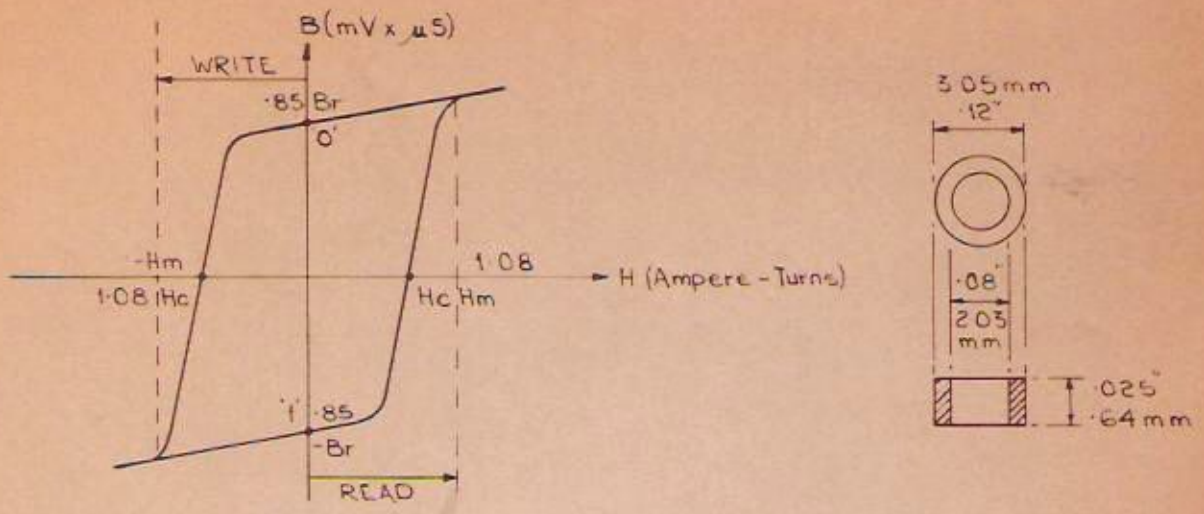
(a) CIRCUIT



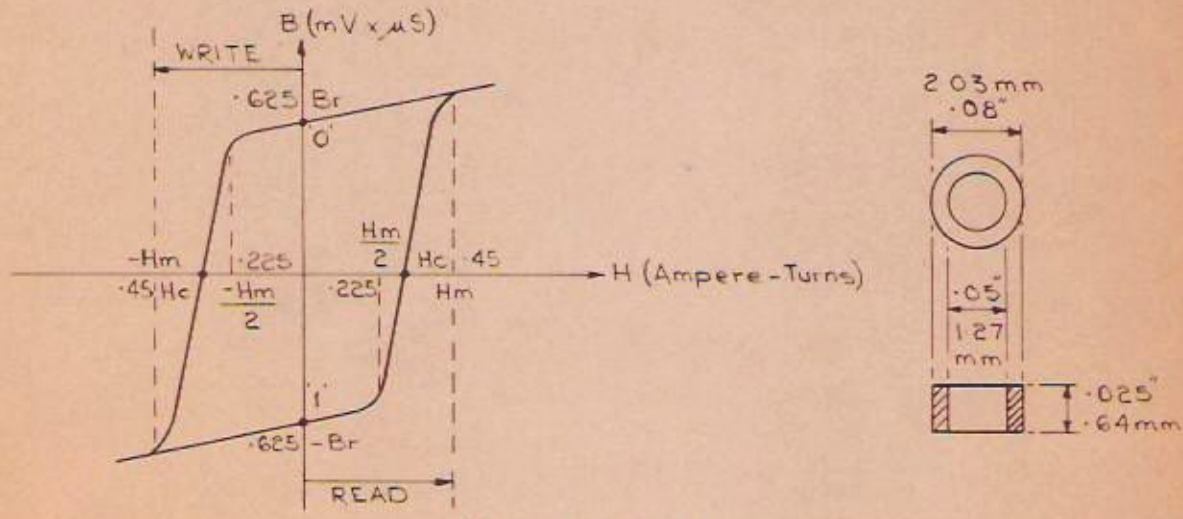
(b) WAVEFORMS

FIG 3 TRIGGER CIRCUIT ON ALL TD BOARDS

FIG 3



(a) LOGIC CORE



(b) STORE CORE

FIG. 4 B/H LOOP AND DIMENSIONS OF CORES

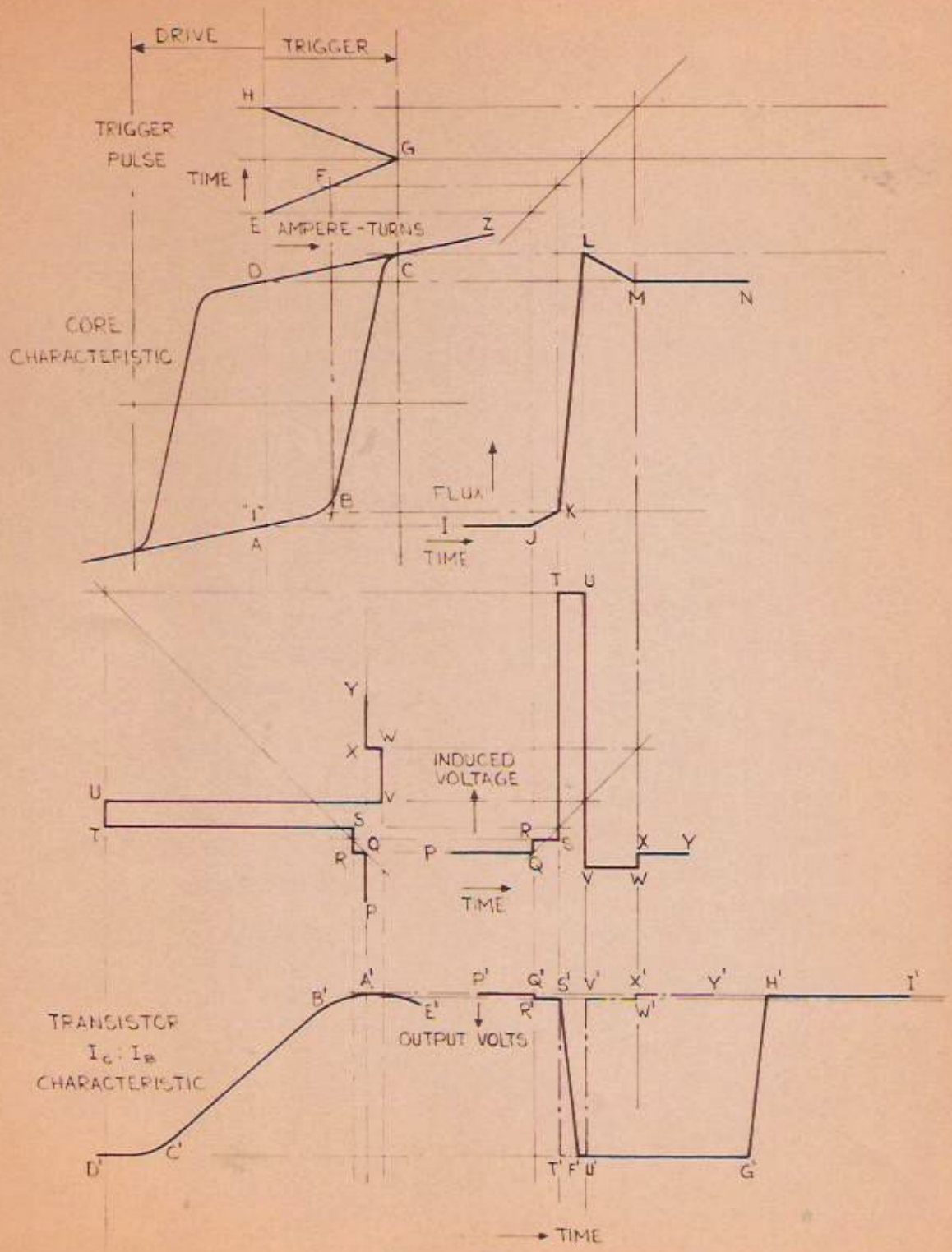
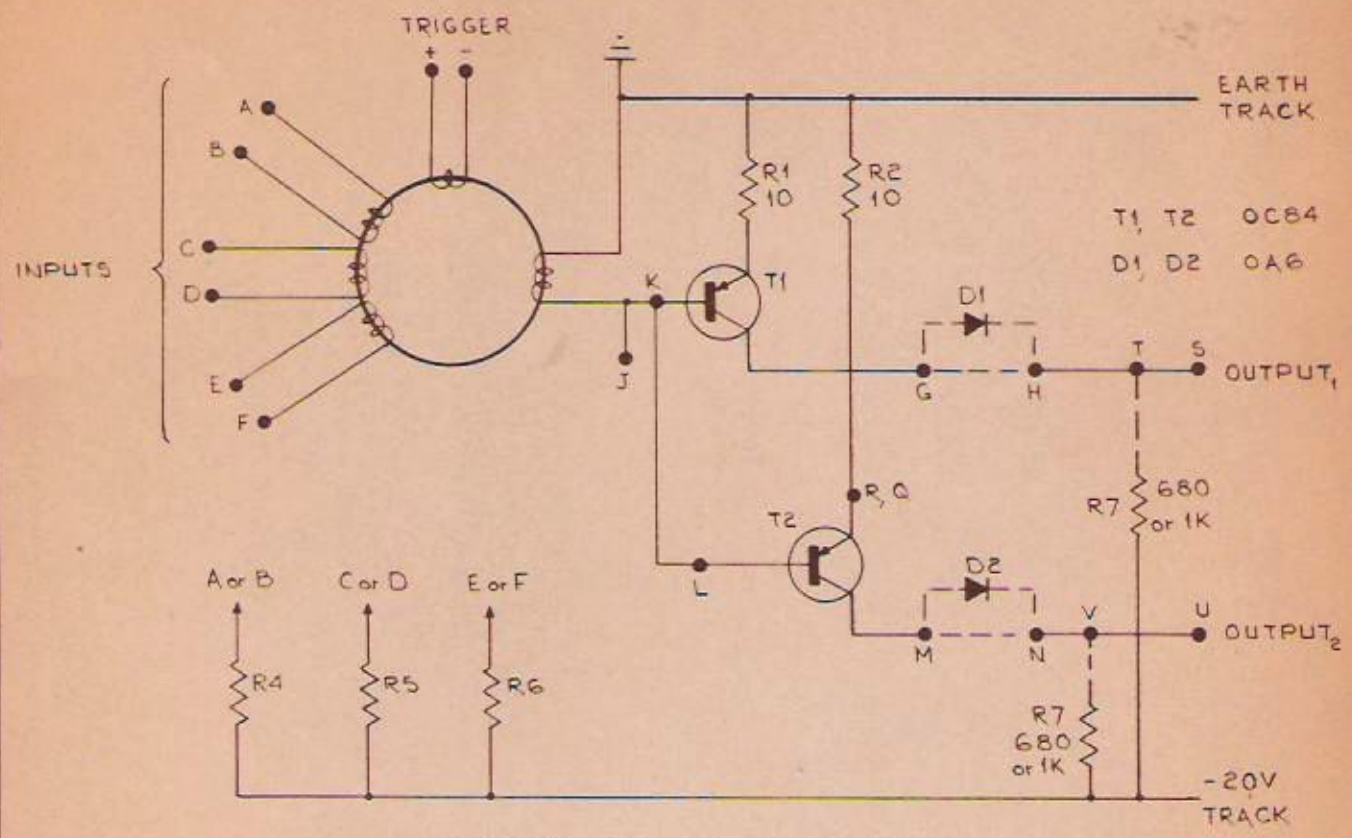
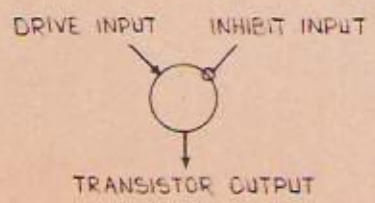


FIG 5 CORE-TRANSISTOR RESPONSE

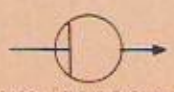
FIG. 5



(a) GENERAL CIRCUIT SCHEMATIC



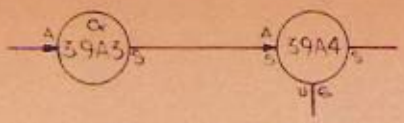
(b) BASIC SYMBOL



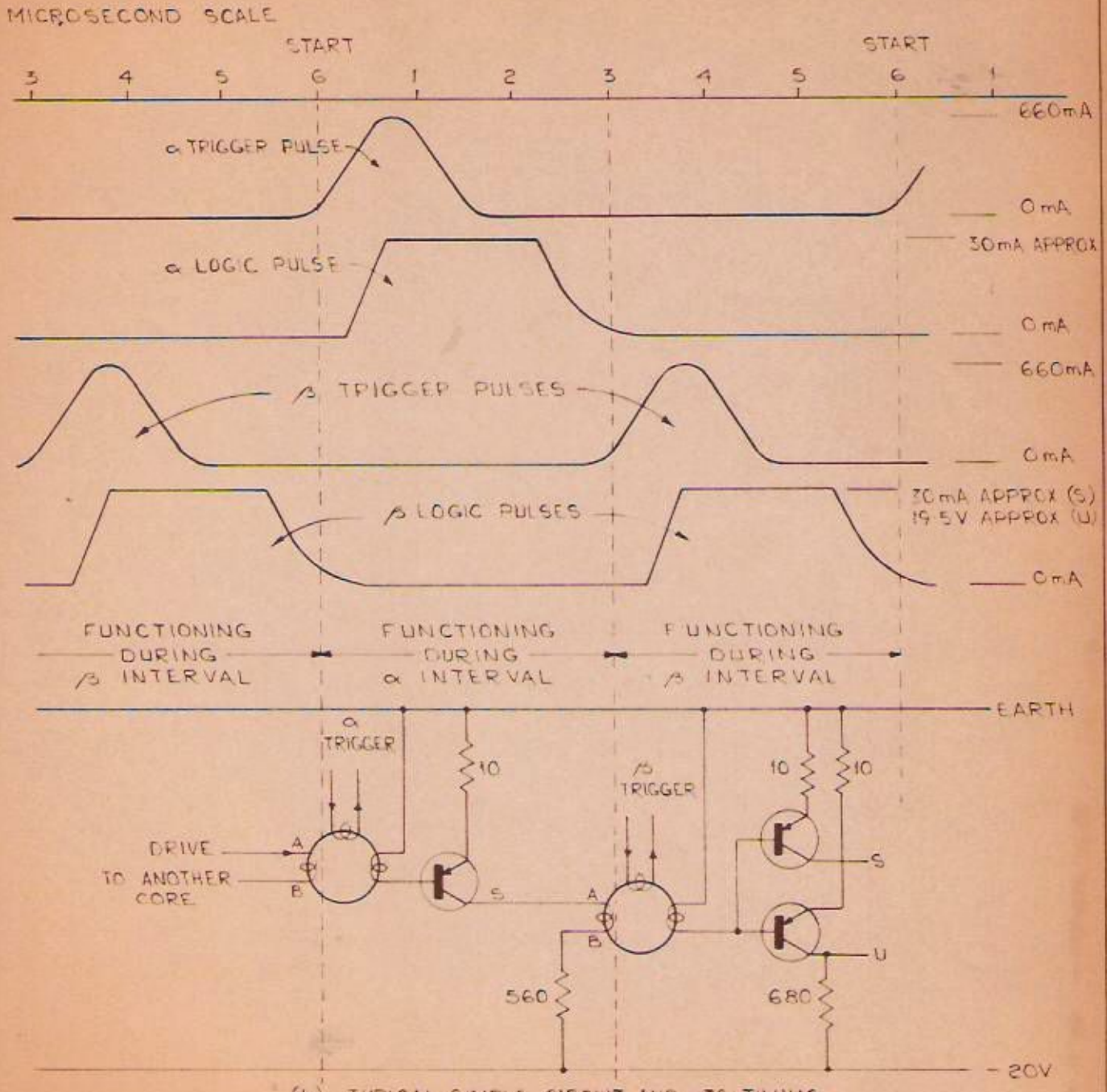
(c) SYMBOL FOR T2 AND ASSOCIATED COMPONENTS USED SEPARATELY

FIG.6 SPI–6 CORE ELEMENTS

FIG. 6



(a) REPRESENTATION OF (b) ON LOGIC DIAGRAM



(b) TYPICAL SIMPLE CIRCUIT AND ITS TIMING

FIG 7 CIRCUIT SYMBOLS AND INTERPRETATION

Transistors T5, T6 and T7 are each transformer-coupled amplifiers, the transformers being damped by resistors in series with diodes to protect the transistors against overload. They amplify the pulse but do not shape it further, apart from some squaring of its peak by driving T7 beyond the limit of its linearity.

Transistor T7 with its associated circuits is representative of five amplifiers each feeding outlets to eleven logic boards. It will be observed that the outlets carry a +0.5V bias in addition to the pulse: it is obtained from the +10V supply via R1 and stabilised by the diodes D1, D2.

2.4 Trigger Generators on Logic Boards

Each logic board has its α and β trigger generating circuits which obtain the required triangular pulse from the shorter square input pulse and give it out with sufficient power to trigger all the cores in its phase on the board. These circuits are at the top of the board, the output transistors being mounted on heat sinks.

Fig.3a shows the circuit. T11, normally cut off by the 0.5V bias on the input, further amplifies the input pulse. R11 limits the base current, preventing prolongation of the pulse by hole storage: C11 enables the sharp leading edge to be retained.

T12 supplies the output power and also, in conjunction with the inductive load, gives the final shape to the pulse. The pulse applied to its base is shown in Fig.3b: it is square, with duration equal to that of the rising front of the output pulse. The emitter is biassed by the charging of C12 during each pulse: as the time constant of C12 and R13 is 37.5 μs the emitter is always strongly negative with respect to the base except during the input pulse. During the input pulse the output transistor is fully conducting, the leading slope of the output pulse being shaped by the inductance of the load in the output circuit. When the input square pulse finishes, the stored holes are swept up under the combined action of the -20V supply and the inductive surge in the load to give the required slope to the trailing edge. The output trigger pulse rises in about 3/4 μs to its peak value of 660 mA and then falls to zero in another 3/4 us.

Resistor R14 is selected on test to ensure that the output pulse is correct and will continue to be correct should any circuit constants vary with temperature and age. It determines the average bias upon T12 emitter.

3. FERRITE CORES

Most of the arithmetic and logic functions of the computer, and the storage of data, are achieved by an application of the magnetic properties of a ferrite, in the form of annular cores.

The ferrite has two kinds of response, one rapid and relatively small and the other slower but larger. They appear to represent changes in electron spin and changes in magnetic domain respectively. It is the slow, strong response that is used, but the small quick response appears in some applications, and the circuits associated with the reading process in the matrix store have to be designed to distinguish between the two kinds of response.

The hysteresis curve of the ferrite is very rectangular. The dimensions are shown in Fig.4 in which the axes of the curves are not marked in units of magnetomotive force and flux density, but in units of ampere-turns and millivolt-microseconds.

It will be seen that a larger core is used for logic and a smaller for the store. With each, if a certain number of ampere-turns is sufficient to reverse the remanent flux (from Br to -Br or from -Br to Br), half that number of ampere-turns causes a practically negligible change in the remanent flux. This phenomenon is of particular importance in the use of cores in the store, where the values are critical.

One condition of remanent flux, marked 0 in the figure, represents the digit that is elsewhere represented by the absence of a pulse: the other condition of remanent flux, marked 1 represents the digit that is elsewhere represented by the presence of a pulse.

Cores are driven by a pulse, if it exists, during one phase of the digit time, and restored to the 0 condition by a trigger pulse during the next phase, and are known by the phase of their trigger pulse. An α core, for example, is driven (if it is to hold a 1) during the β phase of one digit time, and driven back to the 0 condition about 3 μs later by the next α trigger pulse. If the reversal of flux to restore the 0 condition does occur, the change of flux in an output winding is amplified and formed into a pulse suitable for driving subsequent cores. If the core has not had a 1 written into it the trigger pulses causes a very much smaller change of flux, so that the pulse induced in the output winding is too small to produce an output from the associated amplifier. The change of flux during the process of writing a 1 into the core is in the reverse direction, and the pulse thereby induced in the winding merely drives the output amplifier further into the cut-off condition.

3.1 Inhibit Windings

It is frequently convenient to provide an "inhibit" winding which may be energised in the opposite direction to that required to write a 1: if the write pulse occurs while the inhibit winding is energised their opposition produces a zero resultant, so that the core remains in the 0 condition. There is no effective change of magnetisation when the inhibit winding is energised alone as the core is already in the 0 condition.

3.2 Detailed Description of Operation

Fig.5 shows a more detailed analysis of the behaviour of a core with its associated transistor, which acts as a pulse shaper, a buffer stage and an output power amplifier.

It is assumed that a drive pulse during the previous phase (i.e. half-digit time) has changed the remanent magnetism from the condition at D, representing 0, to that at A, representing 1. The trigger pulse has to restore the 1 to a 0 by taking the magnetisation round the curve from A past the points B, C, Z to D. The point Z may vary with external conditions, but the magnetisation must be carried at least to C to achieve saturation. The following explanation has been simplified by assuming that the core characteristic is a parallelogram and that the trigger pulse drives it exactly to C.

The trigger pulse is represented by the triangle EGH, the time base of which has been projected to the right and down the page. At the time E as the pulse starts the magnetisation is at A, and with the sloping leading edge of the pulse the magnetisation rises first to B, corresponding to the point F on the graph of the pulse. The magnetic flux is plotted to the right of the core characteristic: the portion IJ represents the constant condition of A before the trigger pulse began, and the sloping part JK shows the change from A to B. As the trigger pulse continues from F to G the magnetisation changes rapidly from B to C, as shown from K to L on the flux-time graph. As the trigger pulse current falls again from G to H the magnetisation falls from C to D, as shown at LM, and remains at D, representing 0, as shown at MN.

If the load on the output winding were a high ohmic resistance the flux would not be appreciably influenced by the current in the output winding: the current would then be proportional to the rate of change of flux in the core. To simplify the explanation these approximations are used in the figure. The rate of change of flux is shown below in the graph IJKLMN and also to the left on a vertical time scale: they are identically marked PQRSTUVWXY . When the flux is constant,

along IJ, the output is zero at PQ. The relatively gradual rise JK induces the voltage RS: the steeply rising portion KL gives the output TU, and the subsequent fall LM gives the reverse voltage VW. When the pulse has passed and the flux is constant the induced current is zero, as shown at XY.

This current is made to flow through the base of a transistor in the common emitter amplifying circuit to be described below. The collector current-base current characteristic of this is shown at E', A', B', C', D'. With zero base current the transistor is in the cut-off condition A', zero collector current being shown on the output current-time graph to the right at P'Q'. The small base current RS causes a minute output current to flow as shown at R'S'. The major driving pulse TU drives the transistor beyond its linear range B'C' to the bottomed condition at at D': if the output circuit were to respond instantaneously its current would follow the curve T'U' with this pulse, it would follow V'W' with the reversed current VW and would fall to zero with XY at X'Y'. But hole storage causes some delay at the start of the output pulse and considerable delay before it terminates, as shown by the graph S' F' G' H' I'. By the use of suitable circuit constants this pulse is made to continue for about 2.5 μs as required in the logic circuits. It will be observed that for this to fall properly within the correct phase the trigger pulse has to be timed very early in the phase.

3.3 Variations from the above conditions

The trigger pulse will normally drive the core to some point such as Z, beyond C. This would make the rise KL steeper, followed by a slow rise. This makes the induced pulse TU higher but of shorter duration. Although the transistor is bottomed, that is to say that its collector-emitter voltage has fallen to the minimum, the flow of current between the base and the emitter will inject holes, so the output pulse will suffer negligible alteration.

If the core has not previously been driven to the condition representing 1, the trigger pulse will carry it up the characteristic from D to Z and back, giving a change of flux which when differentiated gives the graph PQRS and continues along the RS level until it falls to V and goes to WX and Y as before. The transistor output is in consequence negligible. During the phase allocated to forwards driving, an unopposed inhibit pulse produces an identical effect. The ordinary drive pulse, taking the core from 0 to 1, produces inverted copies of the graphs IJKLMN and PQRSTUVWXY in Fig.5, so that the transistor will be driven by the large pulse further into the cut-off condition.

It has already been mentioned that the trigger pulse will usually drive the core rather beyond the point C in Fig.5, to some undefined point Z. Similarly, when the core is driven from 0 to 1, the drive pulse must be large enough to take the core to saturation, and will normally exceed that value. If the drive reaches several times this value the amount of remanent magnetism when it ceases will still be the same, that which represents "1". An inhibit pulse must be sufficient to prevent a drive pulse from taking the field round the knee of the magnetisation curve; the total effect of two or three simultaneous inhibit pulses may be to reach a point Z several times as far as C from D.

4. THE USE OF CORES FOR LOGIC

The explanation above has considered a core with three or four windings, used as follows:

(a) A pulse in a drive winding may change the remanent magnetisation of the core from the 0 to the 1 condition.

(b) There may be an inhibit pulse in another winding, which being simultaneous with the drive pulse but opposed to it, prevents it from writing a 1 in the core.

(c) In the phase immediately following the drive phase, if the core is in the 1 condition, a pulse in the trigger winding restores it to the 0 condition.

(d) If the trigger pulse does drive the core from 1 to 0, a pulse is thereby induced in the output winding.

In practice, a core has three, four or five windings, three of which are for the trigger, the output and one drive; the others if present can be used for drives or inhibits. The terminals of one, two or three drive or inhibit windings are allocated the letters AB, CD, and EF on circuit diagrams. Logic diagrams show only the letter indicating the terminal to which the input is brought, thus A, C or E will indicate drive inputs to the 1st, 2nd or 3rd windings respectively, and as an input brought to the other end of a winding will act in reverse, B, D or F will indicate inhibit inputs to the 1st, 2nd or 3rd winding respectively. The resulting logical alternatives are given in the following table, in which u represents "up" i.e. pulse or energising present, d represents "down", the no-pulse condition.

(i) One drive A only

A	Output
d	d
u	u

As the output occurs half a digit time later than the input (or in particular circumstances up to one digit time later), this is used to delay pulses.

(ii) One drive A, one inhibit D

A	D	Output
d	d	d
d	u	d
u	d	u
u	u	d

(iii) Two drives, A, C

A	C	Output
d	d	d
d	u	u
u	d	u
u	u	u

(iv) Two drives, A, C, one inhibit F

A	C	F	Output
d	d	d	d
d	d	u	d
d	u	d	u
d	u	u	d
u	d	d	u
u	u	d	u
u	u	u	u*

* This condition is rarely used. Normally, when a core has two drive windings and an inhibit winding, the logic is such that the two drive windings cannot be energised simultaneously. The one case in which this restriction does not apply is in the adder (see Leaflet 43).

(v) One drive A, two inhibits D, F

A	D	F	Output
d	d	d	d
d	d	u	d
d	u	d	d
d	u	u	d
u	d	d	u
u	d	u	d
u	u	d	d
u	u	u	d

(vi) Three drives, A, C, E

A	C	E	Output
d	d	d	d
d	d	u	u
d	u	d	u
u	d	d	u
u	d	u	u
u	u	d	u
u	u	u	u

4.1 Logic Elements and their Circuits

In the space allocated to a logic element one or two output transistors can be accomodated. The available circuit alternatives are shown in the following table. To distinguish the different types of element the cores are potted in material of different colours.

Name of element	Input windings	No. of output transistors	Outputs	Colour
SP1	AB	1	S	Black
SP2	AB, CD	1	S	White
SP3	AB, CD, EF	1	S	Red
SP4	AB	2	S, U	Orange
SP5	AB, CD	2	S, U	Yellow
SP6	AB, CD, EF	2	S, U	Green

4.1.1 Termination

The input windings (drives and inhibits) are in the output circuits of similar elements acting in the preceding phase. One output circuit may include windings on several cores. All the windings in any one circuit are in series, and between them and the -20V supply a terminating resistor is included. A drive winding is loaded by the energy required to change the magnetisation of the core: but an inhibit pulse, or a drive pulse applied to an inhibited core, meets a relatively negligible impedance, because it does not use energy in changing the magnetisation.

The transistor amplifier is designed to match 680Ω at its output, and the core logic input (A, C or E) has an impedance of about 120Ω when the core is driven from 0 to 1. The terminating resistor where the circuit reaches the -20V supply, is usually chosen as follows:

(a) 680Ω if all windings are inhibits.

(b) 560Ω if one winding is a drive.

(c) 430Ω if two windings are drives.

(d) 300Ω if three windings are drives.

However, if two drive windings are on cores one of which must always be inhibited, that is to say on cores one of which is inhibited with a function and the other is inhibited with the inverse function, allowance is made for the load of one drive only. Also, when there is no inhibit winding on a core the opportunity is sometimes taken to over-drive it by using a lower value of terminating resistor: this ensures that if an input pulse should happen to be of reduced magnitude, the output pulse will be of full size.

4.1.2 Circuit Description

Fig. 6a is a generalised circuit schematic. As shown in the table in 4.1 above, transistor T2 and its associated components are omitted from SP1, 2 and 3, although as explained later a transistor used for another purpose may occupy that physical location. Input EF or both CD and EF may be omitted: terminating resistors R4, R5 and R6 are provided only when required. For a normal drive the inputs are brought to A, C and E; B, D and F are then connected to R4, R5 and R6 or to the input windings of other cores. To use a winding to inhibit, the input is brought to B, D or F; in these circumstances A, C or E is connected to the load resistor or to an input winding of another core.

The trigger windings of all the α cores on a logic board are connected in series to the source of α trigger pulses, as already described, and the β trigger windings are similarly connected.

It will be seen that the transistors, which as already explained amplify and shape the output pulse, are connected in the orthodox common emitter configuration, with a resistor of about 10Ω in the emitter circuit, to determine the pulse duration. A winding used to inhibit is connected in the opposite direction to a drive winding, and the voltage when a 1 is being read by a trigger pulse tends to make the collector of its driving transistor positive, so that the transistor becomes merely a conducting rectifier loading the coils. To prevent this undesirable condition when the load includes two or more inhibit windings, blocking diode D1 or D2 is included in series with them. When the diode is not required, G is strapped to H (or M to N).

When the output is required in the form of a voltage pulse, the circuit is completed through the load resistor R7.

Figure 6a includes all the components required for every alternative, some of which are exclusive: most logic elements are very much simpler.

Each element is represented on a logic diagram by a symbol of which Fig.6b shows the components. As already stated, it is known as an α or β core element, according to the phase of its trigger pulse. The α cores are so marked, β cores being unmarked. Each element is named according to the logic board on which it is mounted, and its position on that board. Fig.6c shows the symbol for a transistor used independently of the core occupying the same location on the board. Fig.7a shows an example of the use of symbols, and Fig.7b shows the circuit represented, together with its timing. In Fig.7a the names 39A3 and 39A4 show that the core elements are on logic board 39, column A, positions 3 and 4. On each core the letter A shows that the drive is brought to A. Load resistors are denoted by their "hundreds" digit alone: the 5 on the input to 39A4 therefore shows that B is connected via a 560Ω resistor to the -20V supply. The absence of a number at the input to 39A3 shows that B on that core is connected to another input winding elsewhere. 39A4 has two outputs: current from S, and voltage, across a 680Ω resistor, at U.